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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/083,756

02/25/2002

Do-Hyung Kim

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04/07/2004

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER

VU, QUANG D

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/083,756

Applicant(s)

KIM ET AL.

Examiner

Quang D Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18, 20-22 and 24-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18, 20-22 and 24-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,174,785 to Parekh et al. in view of US Patent No. 6,231,673 to Maeda.

Regarding claims 1 and 12, Parekh et al. (figures 1A-G) teaches a method for forming an oxide layer having a first thickness (the thickness of layers [12] and [16] is about 1050 to 8500 angstroms) in an integrated circuit device process, comprising:

forming the pad oxide layer (12) having a second thickness (thickness of layer [12] is about 50 to 500 angstroms) thinner than the first thickness using a thermal oxidation method (column 4, lines 35-39) on a surface of a semiconductor substrate (10).

forming a CVD material layer (16) having a third thickness substantially equal to a difference between the first thickness and the second thickness on the thermal oxide layer (12).

Parekh et al. differ in not showing forming a thermal oxide layer and a CVD material layer in the same CVD apparatus. However, Maeda (figure 25) teaches conducting processing such as heat treatment, thermal oxidation, and CVD processing (column 15, lines 51-55), a single apparatus, which reads on a CVD apparatus. It would have been obvious to one having ordinary skill in the art at the time the invention was made to conduct thermal oxide growth and CVC

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deposition in the same apparatus as taught by Parekh et al. because it would reduce the processing time and contamination.

Regarding claim 3, Parekh et al. teach the CVD material layer (16) is formed of a material of silicon oxide (column 4, lines 48-55).

3. Claims 2, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al. in view of Maeda, and further in view of US Patent No. 4,804,633 to Macelwee et al.

The disclosures of Parekh et al. and Maeda are discussed as applied to claims 1 and 3 above.

Regarding claim 2, Parekh et al. and Maeda differ from the claimed invention by not showing the thermal oxide layer having a thickness of approximately 20 Angstroms to 100 Angstroms. The thickness of the thermal oxide layer is a known variable, which is subject to routine experimentation and optimization. Macelwee et al. show that it is conventional to form pad oxide with thickness of approximately 100 Angstroms (column 3, lines 39-41), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal oxide layer having a thickness of approximately 20 Angstroms to 100 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 5, Parekh et al. and Maeda differ from the claimed invention by not showing growing a thermal oxide layer using oxygen. The oxygen is a known material for growing a thermal oxide layer. Macelwee et al. show that it is conventional to form thermal

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oxide layer using oxygen (column 3, lines 36-41). It would have been obvious to one having ordinary skill in the art at the time the invention was made for growing a thermal oxide layer comprises using oxygen, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

Regarding claim 6, Parekh et al. and Maeda differ from the claimed invention by not showing growing a thermal oxide layer having a temperature of approximately 750⁰C to 1000⁰C. The temperature of thermal oxide layer is a known variable, which is subject to routine experimentation and optimization. Macelwee et al. show that it is conventional to form thermal oxide layer with temperature of approximately 1000⁰C (column 3, lines 36-41), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for growing a thermal oxide layer having a temperature of approximately 750⁰C to 1000⁰C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al. in view of Maeda, and further in view of US Patent No. 5,994,201 to Lee.

Regarding claim 4, the disclosures of Parekh et al. and Maeda are discussed as applied to claims 1 and 3 above.

Parekh et al. and Maeda differ from the claimed invention by not showing forming another material layer on the CVD material layer. However, Lee (figures 2A-F) teaches forming

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another CVD polysilicon layer (208) on the CVD material layer (206). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee into the method taught by Parekh et al. and Maeda because it protects the device from the external damage. The combined device shows forming another material layer on the CVD material layer in the CVD apparatus.

5. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al. in view of Maeda, and further in view of US Patent No. 6,150,235 to Doong et al.

The disclosures of Parekh et al., Maeda are discussed as applied to claims 1, 3 and 12 above.

Regarding claims 7 and 13, Parekh et al. and Maeda differ from the claimed invention by not showing forming a CVD material layer having a temperature of approximately 700⁰C to 850⁰C. The temperature of oxide layer is a known variable, which is subject to routine experimentation and optimization. Doong et al. show that it is conventional to form oxide layer with temperature of approximately 600⁰C to 800⁰C (column 4, lines 48-51), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a CVD material layer having a temperature of approximately 700⁰C to 850⁰C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

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6. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al. in view of Maeda, and further in view of US Patent No. 5,923,998 to Liu.

The disclosures of Parekh et al. and Maeda are discussed as applied to claims 1 and 3 above.

Regarding claim 8, the combined device teaches the surface of the semiconductor substrate comprises a bottom and a sidewall of a trench (Parekh et al.) formed by etching the substrate to a predetermined depth.

Parekh et al. and Maeda differ in not showing the CVD material layer is formed to a thickness of approximately 50 Angstroms to 400 Angstroms. The thickness of oxide layer is a known variable, which is subject to routine experimentation and optimization. Liu shows that it is conventional to form oxide layer with thickness of approximately 50 Angstroms to 200 Angstroms (column 3, lines 17-20), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the CVC material layer is formed to a thickness of approximately 50 Angstroms to 400 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 9, Parekh et al. teach the CVD material layer (16) is formed of a material of silicon oxide (column 4, lines 48-55).

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7. Claims 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al., Maeda, Macelwee et al. in view of Liu, and further in view of US Patent No. 6,150,235 to Doong et al.

Regarding claims 10 and 14, Parekh et al., Maeda, Macelwee et al., Liu and Doong et al. apply to these claims as discussed regarding claims 1-9 and 12 above.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al., Maeda, Liu, US Patent No. 6,180,493 to Chu in view of US Patent No. 6,140,208 to Agahi et al., and further in view of US Patent No. 5,665,633 to Meyer.

The disclosures of Parekh et al., Maeda and Liu are discussed as applied to claims 8-9 above.

Parekh et al., Maeda and Liu differ in not showing forming a nitride liner layer on the oxide layer. However, Chu (figures 2A-G) teaches forming a nitride liner layer (214) on the oxide layer (212). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chu into the method taught by Parekh et al. and Maeda because it prevents oxidation on the sidewalls of the trench.

Parekh et al., Maeda, Liu and Chu differ in not showing forming a nitride line layer having a thickness of approximately 30 Angstroms to 100 Angstroms. The thickness of nitride liner is a known variable, which is subject to routine experimentation and optimization. Agahi et al. show that it is conventional to form nitride liner with thickness of approximately 55 Angstroms (column 3, lines 30-31), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a nitride

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line layer having a thickness of approximately 30 Angstroms to 100 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Parekh et al., Maeda, Liu, Chu and Agahi et al. differ in not showing forming a trench filling layer having a thickness of approximately 3000 Angstroms to 10,000 Angstroms. The thickness of trench filling layer is a known variable, which is subject to routine experimentation and optimization. Meyer shows that it is conventional to form a trench filling layer of approximately 4000 Angstroms (column 1, lines 32-40), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made forming a trench filling layer having a thickness of approximately 3000 Angstroms to 10,000 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

9. Claims 15, 18, 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,140,208 to Agahi et al. in view of US Patent No. 6,231,673 to Maeda.

Regarding claims 15 and 22, Agahi (figures 5-6) teaches a method of forming a layer for an integrated circuit device, comprising:

forming a trench (17) in a single silicon substrate (10) by etching;

forming an oxide layer of a double layer (20, 23) structure with a first thickness (the thickness of layers [20] and [23]) on a surface of the trench (17);

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forming a nitride liner layer (43) on the oxide layer (20, 23), wherein forming the oxide layer comprises:

forming a oxide layer (23) having a second thickness (the thickness of layer [23]) on the trench (17);

forming a conformal liner material layer (20) having a third thickness substantially equal to a difference between the first thickness and the second thickness on the thermal oxide layer (20); and

forming a trench isolation material (47) on the nitride liner layer (43) to fill the trench (17).

Agahi et al. differ from the claimed invention by not showing the thermal oxide layer, the liner material layer, and the nitride liner layer are formed in the same chemical vapor deposition (CVD) apparatus. However, Maeda (figure 25) teaches conducting processing such as heat treatment, thermal oxidation, and CVD processing (column 15, lines 51-55), a single apparatus, which reads on a CVD apparatus. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Maeda into the method taught by Agahi et al. because it would reduce the processing time and contamination.

Regarding claim 18, Agahi et al. teach the liner material (20) is made of silicon oxide (column 5, line 45). Agahi et al. differ from the claimed invention by not showing the liner material layer is made of silicon dioxide. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the liner material layer is silicon dioxide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

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Regarding claim 26, Agahi et al. teach the liner material (20) is made of silicon oxide (column 5, line 45).

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi et al. in view of Maeda, and further in view of US Patent No. 4,804,633 to Macelwee et al.

Regarding claim 16, the disclosures of Agahi et al. and Maeda are discussed as applied to claims 15 and 18 above.

Agahi et al. and Maeda differ from the claimed invention by not showing the thermal oxide layer is formed to a thickness of 20 Angstroms to 100 Angstroms. The thickness of the thermal oxide layer is a known variable, which is subject to routine experimentation and optimization. Macelwee et al. show that it is conventional to form pad oxide with thickness of approximately 100 Angstroms (column 3, lines 39-41), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal oxide layer having a thickness of approximately 20 Angstroms to 100 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi et al. in view of Maeda, and further in view of US Patent No. 6,174,785 to Parekh et al.

Regarding claim 17, the disclosures of Agahi et al. and Maeda are discussed as applied to claims 15 and 18 above.

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Agahi et al. and Maeda differ from the claimed invention by not showing the liner material layer having a thickness of 50 Angstroms to 400 Angstroms. The thickness of the oxide liner is a known variable, which is subject to routine experimentation and optimization. Parekh et al. show that it is conventional to form oxide liner with thickness of approximately 100 Angstroms to 200 Angstroms (column 6, lines 21-22), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the liner material layer is formed to a thickness of 50 Angstroms to 400 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

12. Claims 20, 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi et al. and Maeda in view of US Patent No. 4,804,633 to Macelwee et al., and further in view of US Patent No. 6,150,235 to Doong et al.

Regarding claims 20 and 25, the disclosures of Agahi et al. and Maeda are discussed as applied to claims 15 and 18 above.

Agahi et al. and Maeda differ from the claimed invention by not showing forming a CVD material layer is carried out using N_2O and SiH_4 as source gases. Agahi et al. and Maeda are silent with respect to how the CVD material layer is deposited. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a CVD material layer is carried out using N_2O and SiH_4 as source gases, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its

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suitability for the intended use. In re Leshin, 125 USPQ 416. It is known in the art as shown for example by US Patent No. 6,074,917 to Chang et al. (column 4, lines 36-49).

Agahi et al. and Maeda differ in not showing the thermal oxide layer is formed using O₂ at a temperature of approximately 750⁰C to 1000⁰C. The temperature of thermal oxide layer is a known variable, which is subject to routine experimentation and optimization. Macelwee et al. show that it is conventional to form thermal oxide layer with temperature of approximately 1000⁰C (column 3, lines 36-41), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal oxide layer is formed using O₂ at a temperature of approximately 750⁰C to 1000⁰C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Agahi et al., Maeda and Macelwee et al. further differ in not showing forming a CVD material layer having a temperature of approximately 700⁰C to 850⁰C. The temperature of oxide layer is a known variable, which is subject to routine experimentation and optimization. Doong et al. show that it is conventional to form oxide layer with temperature of approximately 600⁰C to 800⁰C (column 4, lines 48-51), which is in the claimed range. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a CVD material layer having a temperature of approximately 700⁰C to 850⁰C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

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Regarding claim 21, the combined device shows forming a trench isolation material (Agahi et al.; 47) on the nitride liner layer (Agahi et al.; 43) to fill the trench (Agahi et al.; 17) in the same CVC apparatus.

13. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi et al. and Maeda in view of Macelwee et al., and further in view of US Patent No. 6,174,785 to Parekh et al.

Regarding claim 24, Agahi et al., Maeda, Macelwee et al. and Parekh et al. apply to this claim as discussed regarding claims 15-18 above.

Response to Arguments

14. Applicant's arguments with respect to claims 1-18, 20-22 and 24-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
March 31, 2004

Quang D Vu
Primary Examiner
